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Investigation of Impactors on Cell Degradation Inside Planar SOFC Stacks

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Abstract

The impactors on cell degradation inside planar SOFC stacks were investigated using both coated and uncoated Fe–16Cr alloys as the interconnects under stable operating conditions at 750 °C and thermal cycling conditions from 750 to 200 °C. It was found that cell degradation inside the stack is primarily dependent on the interfacial contact between the cathode current-collecting layer and the interconnect. Additionally, cell degradation is found to be independent of the high-temperature oxidation and Cr vaporization of the interconnects during stack operation, as the stacks are well sealed. The coating on the interconnect can further improve the contact between the cell cathode and the interconnect when the latter is properly embedded into the current-collecting layer.

Keywords: Cell Degradation, Contact, Impactors, Solid Oxide Fuel Cells, Stack

1 Introduction

The stack lifetime is one of the most important factors in the commercialization of planar SOFCs, generally considered to be affected by the sealing performance, the performances of single cells and interconnects, and the contact between components because the stack is composed of sealing materials, single cells, and interconnects [1, 2]. It is well known that the sealing material choice is the most important factor in cell degradation inside planar SOFC stacks during operation [3]. To maintain the stack sealing performance, a CAS-I sealant was developed and a multi-layer structure sealant was designed in our lab [4]. An OCV >1.1 V was obtained, and the structure remained stable with our self-developed sealant, indicating that an excellent sealing performance was achieved in the SOFC stacks. As the stack was sealed well, the performance of the single cell was identified as the second most important factor in cell degradation. To decrease the degradation rate of the SOFC stack, a low single cell degradation rate is required. Therefore, significant effort has been focused on the improvement of performance in single cells [5–9]. However, the stack degradation is generally significantly reduced by using high-performance single cells [10–12]. Hence, researchers are now focused on studies of metal interconnects as related to cell degradation inside SOFC stacks [13–15]. It was reported that the high-temperature oxidation of metal interconnects and the vaporization of Cr from the metal interconnect poisoning cell cathode affected the cell degradation during stack operation [16–18]. However, no direct relationship between the cell degradation and the performance of the metallic interconnect has been determined [19]. Even so, to prohibit the metal interconnect from affecting the cell degradation, dense protective layers generally have been coated on the surfaces of the metal interconnects [20, 21]. However, the stack degradation rates were still higher than the required value for SOFC commercialization.

Researchers have come to realize that the contacts between metal interconnects and cell electrodes are the most important factor in the stack output performance of planar SOFCs [22–25]. In 2003, Jiang et al. [22] found that the performance increases by more than 7.5 times after the contact area is increased from 4.6 to 27.2% by the addition of silver or platinum mesh on the cathode side. In our group, Guan et al. [26] also investigated the effect of the contact between electrodes and metal interconnects on the stack output performance by designing different contact methods, and we found that the stack output performance is independent of the contact on the anode side but is primarily dependent on the contact between the cell cathode and the cathode side of the interconnect channel tips. Additionally, Yang et al. [24] found that the area specific resistance (ASR) of the interconnect–cathode interface as a function of time can be stably maintained if the contact between the components is significantly improved. These investigations reveal that the stack output power density and the degradation behavior can be significantly

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improved by optimizing the contact between the metal interconnects and the cell cathodes.

Ultimately, it has been demonstrated that the interconnect and the contact between the components on the cathode side are the two key factors affecting cell degradation inside the planar SOFC stack during operation. However, to the best of our knowledge, the degree of impact of the above factors on cell degradation during stack operation has not been sufficiently clarified. The aim of this work is to reveal the relationship of the metal interconnect and the contact between the interconnect and the cell cathode with the cell degradation behavior inside the planar SOFC stack.

2 Experimental Procedures

The two-cell stack was assembled as shown in the schematic diagram in Figure 1. The stack was composed of three interconnects, several slices of sealant, and two patches of individual planar SOFC single cells. The interconnects used were a commercial SUS430 stainless steel with the composition listed in Table 1. The three interconnects were named interconnects A, B, and C in this work. A channel feature was designed on either side of each interconnect as a gas flow path. The depth of each channel was sufficient for gas to flow smoothly even the channel tip is completely embedded into the cathode current-collecting layer. Interconnects A and B were uncoated, and interconnect C was coated. To ensure a dense coating on interconnect C, plasma spraying technology was used to deposit a composite coating of microspherical powders of $Ni_{80}Cr_{20}$ and $(La_{0.75}Sr_{0.25})_{0.95}MnO_3$ (LSM). The $Ni_{80}Cr_{20}$ powders were sprayed on the interconnect first, followed by spraying of the LSM powders. The sealant used in the current work was a self-developed type of Al_2O_3–SiO_2–CaO-based material [4]. The coefficient of thermal expansion (CTE) was approximately equal to that of the YSZ electrolyte. The sealing structure was configured and pasted on both sides of the interconnect to ensure proper stack sealing performance.

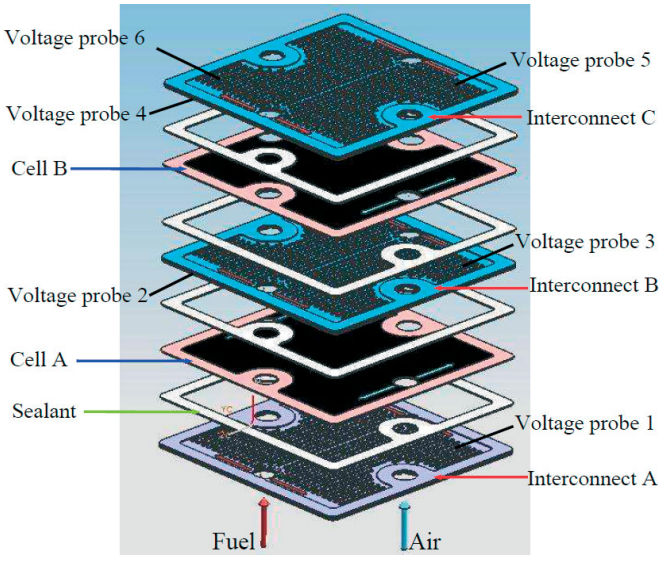

Fig. 1 Schematic diagram of stack assembly and probe locations in stack.

Table 1 Chemical composition of SUS430 stainless steel.

Elements / wt%	Fe	Cr	Ni	C	Mn	Si	P	S
Interconnect B	Bal.	16.14	0.044	/	0.209	0.279	0.028	/

The typical anode-supported SOFCs were used as the stack cells with fabricated Ni-YSZ/YSZ/LSM stacks. The cells used in the assembled stacks were denoted as either cell A or cell B. Both cells A and B measured 10 cm × 10 cm in area with an active area of 70 cm^2. A 100-µm-thick current-collecting layer of LSM was coated onto each cell cathode by screen printing. To fabricate the stack, the cathode side of cell A was brought in contact with uncoated interconnect B, and the cathode side of cell B was brought in contact with coated interconnect C. Porous nickel was placed on the anode side of both cells A and B for use as an anode current collector. The contact area between each interconnect and each cell electrode measured 25% of the cell active area. Cell A with interconnect B and cell B with interconnect C were named stack units 1 and 2, respectively.

To measure the voltage drop caused by the components during stack discharging, voltage probes were spot-welded to both sides of the each interconnect using the method reported in the literature [24, 27]. The probe positions are shown in Figure 1. During stack testing, an insignificant voltage difference was found between probes 5 and 6, which were located on the same interconnect surface, indicating that the method applied here to measure the voltage is feasible. The voltage changes induced by the cell and the interconnect in each stack were recorded with the voltage probes. The effects of the coated and uncoated metallic interconnects on stack degradation were analyzed using the corresponding voltage curves. After assembly, each stack was placed in a furnace and heated to 850 °C. To ensure proper sealing, an external weight was loaded onto the stack during the annealing process. Pure hydrogen (99.9%) was flowed at a rate of 7 sccm cm^{-2} into the stack anode channel through the fuel inlet pipe. The NiO-YSZ supported anode was reduced by H_2 for more than 2 h at 850 °C. Compressed air was then introduced into the stack cathode channel at a flow rate of 18 sccm cm^{-2} through the oxidizing gas pipe. The flow directions of fuel and air introduced into the stacks are shown in Figure 1.

Subsequently, the stack degradation and cell degradation inside the planar SOFC stacks were tested under both stable operating conditions at 750 °C and thermal cycling conditions from 750 to 200 °C. The operating conditions of each thermal cycle can be divided into two stages. The first stage involved cooling from 750 to 200 °C, followed by holding at 200 °C for more than 5 h. The second stage involved heating from 200 to 750 °C, followed by holding at 750 °C for more than 15 h. A direct current (DC) of 7 A was discharged at long-term stable operating conditions, and 6 A direct current was discharged every thermal cycle while maintaining the temperature at 750 °C. The length of each thermal cycle was 50 h.

To determine the factors that caused cell degradation inside the SOFC stacks, scanning electron microscopy (SEM; Hitachi S-4800) and energy dispersive X-ray spectrometry (EDS) were used to diagnose the morphology and elemental distribution in the middle region of each cell and interconnect. After testing, the elemental distribution within the various layers of the cells and interconnects inside the stacks were quantitatively analyzed using X-ray fluorescence (XRF; Rigaku ZSX Primus II) spectrometer and inductively coupled plasma-atomic emission spectrometry (ICP-AES; Perkin-Elmer Optima 2100).

3 Experimental Results and Discussion

3.1 Stack Degradation Under Stable Operating Conditions

Figure 2 shows the *I–V* curves and durability curves of both types of two-cell stacks under stable operating conditions at 750 °C. It can been observed that the average open circuit voltages (OCVs) of the stacks were all more than 2.2 V, which indicates good sealing performance in the stack. The maximum output densities of stacks 1 and 2 reached 0.11 and 0.14 W cm^{-2}, respectively. The original performance of stack 1 was lower than that of stack 2. After each *I–V* test curve was collected, the stack was discharged at a 0.1 A cm^{-2} direct current with a fuel utilization of approximately 10%. The degradation rates of stacks 1 and 2 reached 0.86% per 100 h and 1.18% per 100 h, respectively. The degradation rate of the two-cell stack was significant under the conditions used in the current work.

Figures 3 and 4 show the *I–V* curves and durability curves of the components of both two-cell stacks. The OCVs of the cells in stacks 1 and 2 both reached values >1.1 V based on Figures 3a and 4a, respectively. The output power densities of cells A and B in stack 1 reached 0.09 and 0.13 W cm^{-2}, respectively. The deterioration behavior of the single cell and the stack unit in stack 1 can be divided into two stages, including the activation and degradation stages. The degradation rate of cell A and stack unit 1 reached 0.92% per 100 h, whereas that of cell B and stack unit 2 only reached 0.77% per 100 h. The degradation behavior of cell A and stack unit 1 in stack 2 also can be divided into two stages. Unlike stack 1, the first stage involved rapid degradation at the rate of 3.21% per 100 h. In the second stage, the degradation was slightly slower (0.25% per 100 h). The degradation behavior of cell B and stack unit 2 in stack 2 can be divided into three stages, including activation, stable operation, and degradation, with an overall degradation rate of 2.27% per 100 h. From Fig-

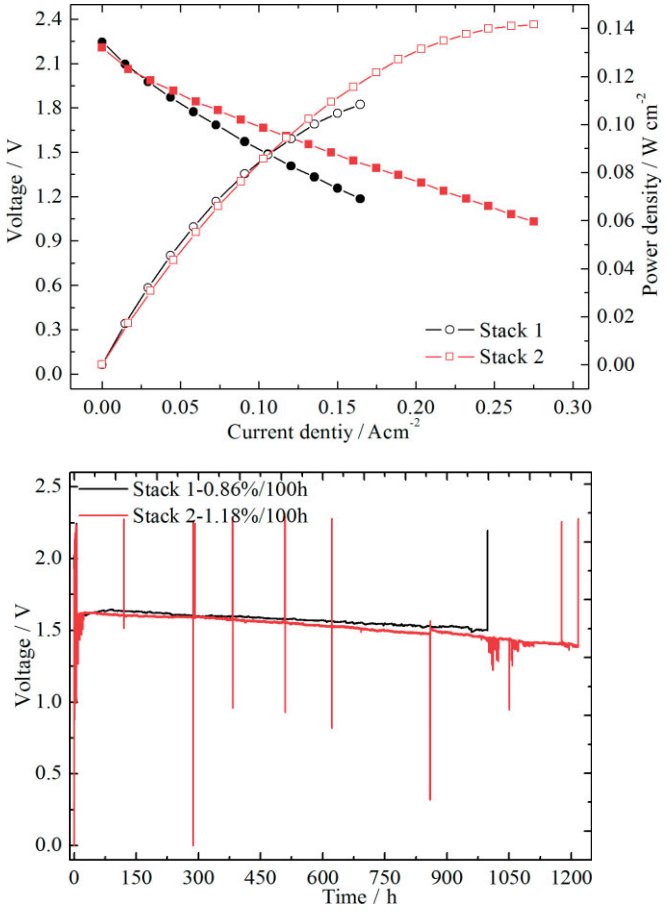

Fig. 2 Durability tests of stacks at 750 °C under 0.1 A cm^{-2} discharging current.

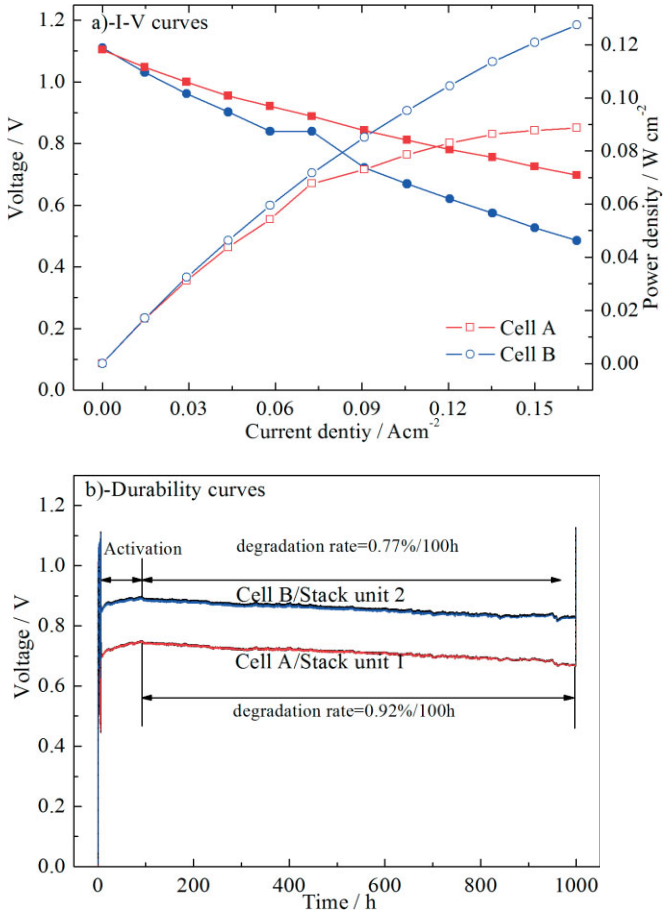

Fig. 3 *I–V* curves and durability curves of stack 1: (a) *I–V* curves and (b) durability curves.

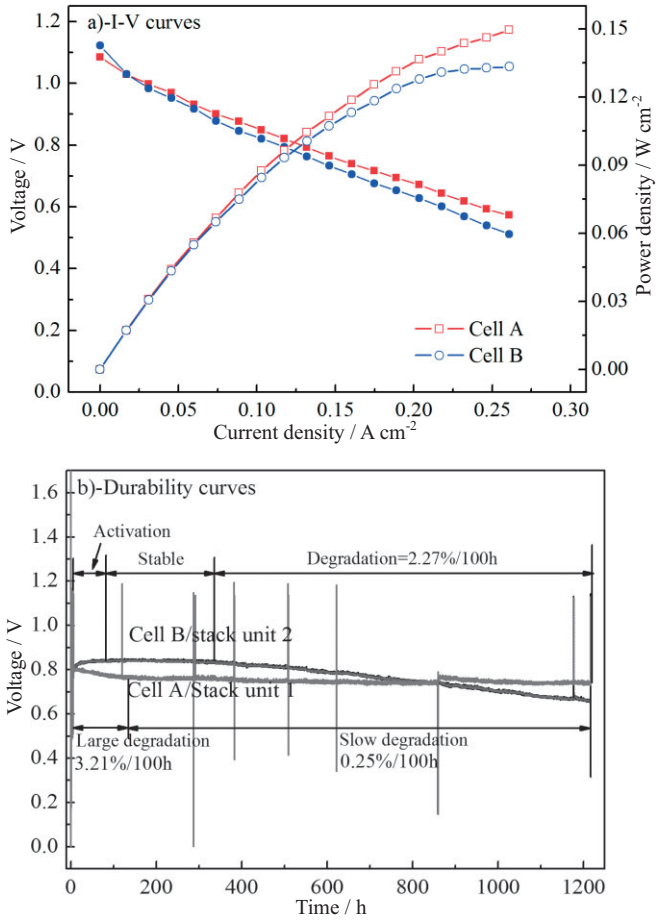

Fig. 4 *I–V* curves and durability curves of stack 2: (a) *I–V* curves and (b) durability curves.

ure 4a, it can be observed that the output power density of cells A and B in stack 2 reached 0.13 and 0.15 W cm^{-2}, respectively. However, the cell performance values recorded here were significantly lower than those reported in the literature [25, 26]. Based on these results, the degradation rate of the cell apparently decreased with increasing output power density.

Figures 3b and 4b show that the degradation rate of the entire stack unit was approximately equal to that of its corresponding cell, which indicates that the ASR of the interconnect was very small and remained stable. The ASR of the interconnect can be calculated by the following formula [28]

$$\mathrm{ASR} = \frac{V_{\text{stack unit}} - V_{\text{cell}}}{I} S \qquad (1)$$

$V_{\text{stack unit}}$ and V_{cell} represent the voltage induced by the stack unit and the cell during discharging, I represents the discharging current, and S represents the active area of the cell. The voltages induced by stack units 1 and 2 during discharging are recorded as the voltage drops between probe 1 and probe 3 (V_{13}) and between probe 3 and probe 5 (V_{35}), respectively. The voltages induced by cells A and B are the voltage drops recorded between probes 1 and 2 (V_{12}) and probes 3 and 4 (V_{34}), respectively. Therefore, the ASRs of interconnects B and C can be calculated based on Eq. (1) as

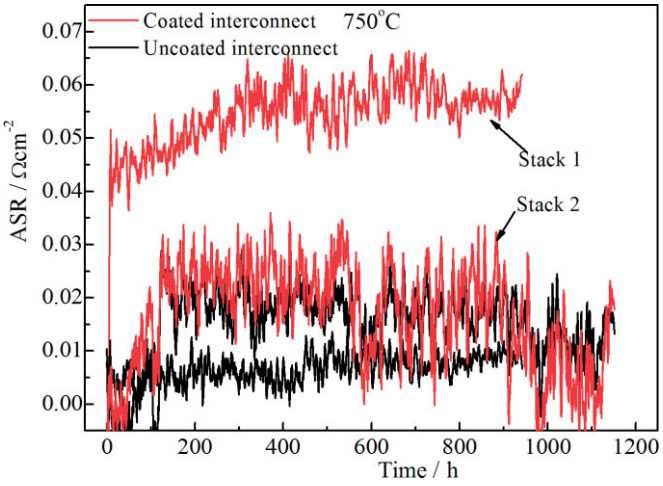

Fig. 5 The ASR of uncoated and coated interconnect under stack stable operation.

$(V_{12} - V_{13}) \times S/I$ and $(V_{34} - V_{35}) \times S/I$, as shown in Figure 5. The ASR of the uncoated interconnect in stack 1 remained stable at 10 mΩ cm^{-2}. However, the ASR of the coated interconnect increased from 40 to 60 mΩ cm^{-2} within 400 h and then remained stable at 60 mΩ cm^{-2}. The ASRs of the uncoated and the coated interconnect in stack 2 always remain less than 20 mΩ cm^{-2}. The ASR of the coated interconnect in stack 2 was significantly less than that in stack 1 due to the plasma spraying. The ASR of the uncoated interconnect in stack 2 was approximately equal to that of stack 1.

These ASR results indicate that the oxidized layer on the uncoated interconnect, achieved under a high-temperature oxidizing atmosphere, has an acceptable and stable electrical conductivity. The ASR of the uncoated Fe–16Cr alloy interconnect during actual stack operation varied from that obtained under the simulated environment [29]. The ASR of the coated interconnect in stack 2 was found to be approximately equal to that of the uncoated interconnect, demonstrating that the coating layer applied on the interconnect also had a very low ASR and remained stable during operation. Additionally, the high-temperature oxidation of the uncoated interconnect caused an insignificant degree of voltage drop, indicating that the oxidation had little effect on the stack degradation. The results of the current work also differ from that of a previously published investigation [30], wherein oxidation on the cathode side of the uncoated interconnect was found to cause one-third of the total stack degradation. In that study, the ASR of the oxide scale growth was measured on ferritic alloys during stack operation under a simulated atmosphere. Therefore, the contributions of the interconnect oxide scales to stack degradation could not be detected in the actual stacks, although such contributions are measurable in the simulated stack environments.

The diffusion of Cr into the cell cathode from the Fe–Cr-based alloy metallic interconnects can cause rapid and serious degradation [30, 31]. The degradation rate of stack unit 1 and cell A in stack 1 was 0.15% per 100 h higher than that of stack unit 2 and cell B. In contrast, the degradation rate of stack unit

1 and cell A in stack 2 was 2.02% per 100 h lower than that of stack unit 2 and cell B. This result indicates that either only a small amount of Cr vaporized from the uncoated interconnect deposits in the cathode or that the presence of Cr did not affect the stack degradation even when deposited in the cell cathode.

The morphology of the interconnect after stack testing and a corresponding EDS linescan are shown in Figure 6. A thickness range of 13–15 µm and 2 µm of oxide layer can be identified on the cathode and anode sides of the uncoated interconnect. The thickness of the oxide layer on the anode side is 13.3–15.4% that of the cathode side. The total growth rate v of the oxidation layer on both sides of the Fe–16Cr alloy interconnect can be obtained from:

$$v = \frac{x_{\text{cathode}} + x_{\text{anode}}}{t_{\text{oxidation}}} \quad (2)$$

where x_{cathode} and x_{anode} denote the oxidation thicknesses on the cathode and anode sides, and $t_{\text{oxidation}}$ represents the operation time. Consequently, the growth rate v of interconnect B is calculated to be 0.0123 µm h^{-1}. Interconnect B (with a thickness of 1.5 mm) requires more than 100 000 h to be oxidized completely. The lifetime of the alloy in the current study is twice that of the current SOFC stack requirement.

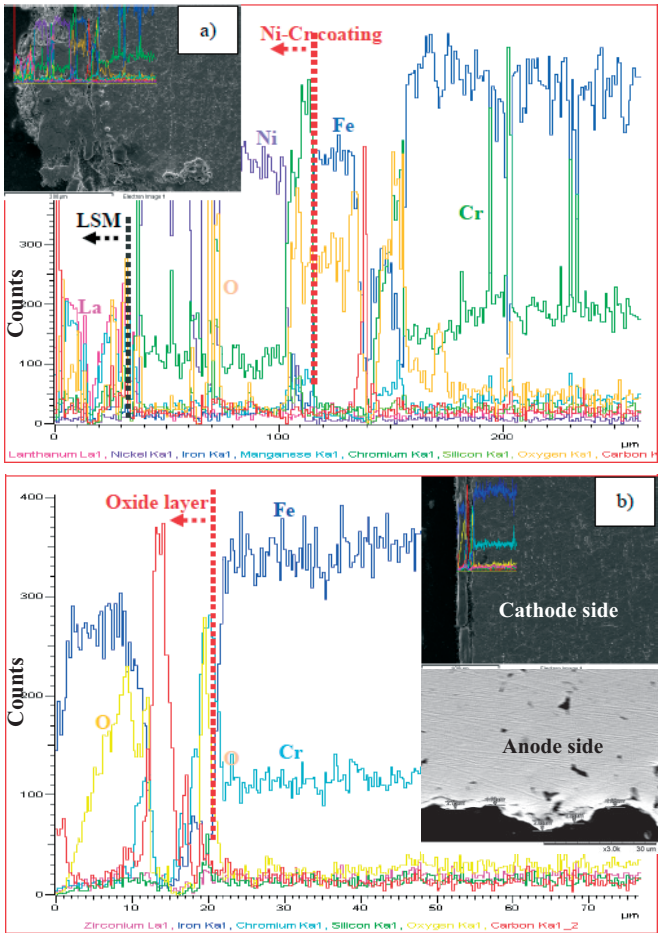

Fig. 6 The morphology and EDS line of interconnect: (a) coated and (b) uncoated.

The EDS linescan of the coated interconnect in Figure 6a shows that insignificant quantities of Cr and Fe have diffused into the coated layer, implying that the coating can effectively protect the surface from oxidation and elemental diffusion. With respect to the uncoated interconnect, it can be clearly observed that both Fe and Cr are present in the oxide layer, and the content of Fe is significantly higher than that of Cr. To quantitatively determine the contents of each element accurately, XRF was applied. The measured data are listed in Tables 2 and 3 and show that approximately 6.67 and 1.54 wt.% Cr exist within the oxidation layer of interconnect B and the LSM protective layer of interconnect C, respectively. The identification of Cr and Ni within the LSM coating layer of interconnect C indicates that the protective LSM coating layer is not sufficiently dense in this work. Fe is the primary element that has diffused into the oxide layer on the cathode side of the uncoated interconnect, while only a small quantity of Cr appears in the oxide layer. This finding reveals a faster rate of oxide scale growth than that reported by Kurokawa et al. [18] and Brylewski et al. [32]. However, based on Figure 5, the overall ASR of the uncoated and coated interconnects almost always remains stable throughout the stack operation. Therefore, it can be concluded that the interconnect coating has an insignificant effect on cell degradation inside the stack by increasing the ASR by oxidation.

To determine the effect of Cr on cell degradation, the distribution of Cr on the cathode side of the cell was quantitatively analyzed by EDS in the line scanning mode, as shown in Figure 7. It can be observed that the distribution of Cr on the cell cathode side is relatively homogeneous, particularly at the interface on the cathode side of the cell, indicating that an insignificant amount of Cr diffused into the cell cathode side under stack operation. Further, to confirm the quantity of Cr in the cell cathode with increased accuracy, the elemental distribution in the cathode side of cells A and B was also measured by ICP-AES, and the data are given in Table 4. It has been reported that Cr can poison the LSM-YSZ cell cathode by the formation of Cr_2O_3 and $(Cr, Mn)_3O_4$ at the active triple phase boundaries [33]. It can be observed that 0.022 and 0.033 wt.% of Cr were deposited in the active layers of cells A and B in stack 1 with corresponding cell degradation rates of 0.92% per 100 h and 0.77% per 100 h. Additionally, 0.070 and 0.028 wt.% of Cr was found in the active layers of cells A and B in stack 2 with corresponding degradation rates of 0.25% per 100 h and 2.27% per 100 h. Accordingly, the cell degradation rate in the stacks appears to have had no direct relationship to the Cr content, which is perhaps due to the small

Table 2 Main element in oxidation layer of uncoated interconnect B.

Elements	Fe	Cr	Mn	Si	Others
Wt.%	91.0	6.67	1.41	0.29	0.63

Table 3 Main element in coated layer of coated interconnect C.

Elements	La	Sr	Mn	Ni	Cr
Wt.%	52.3	26.3	12.0	5.37	1.54

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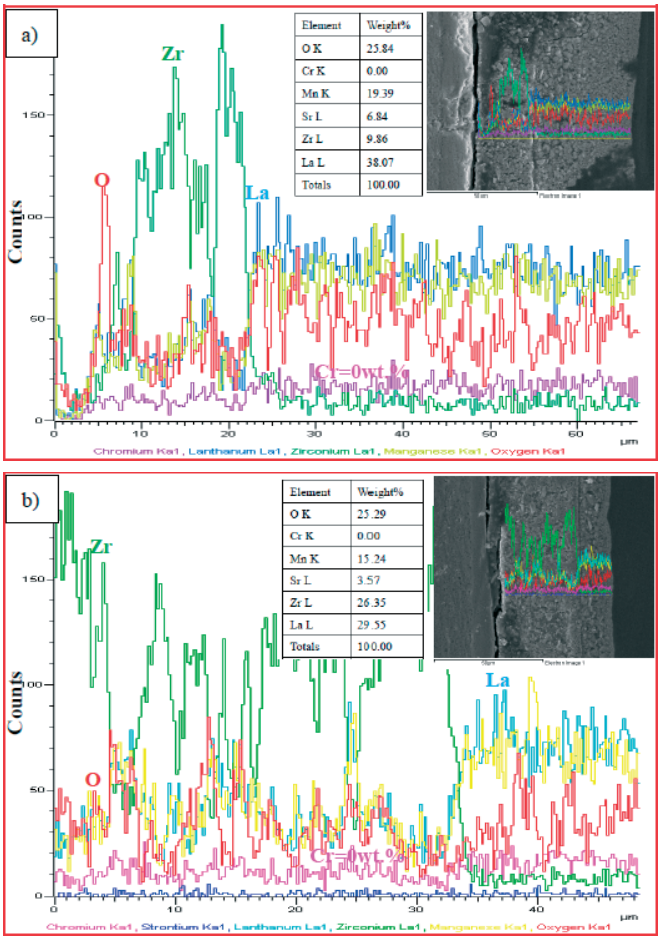

Fig. 7 The morphology and EDS line of cell: (a) cell A and (b) cell B.

Table 4 The content of Cr element in various cathode layer for cells A and B in stack 1 and 2.

Stacks	1 / wt.%		2 / wt.%	
Cells	A	B	A	B
Active layer	0.033	0.022	0.070	0.028

quantity of Cr in the cell active layer in this work; this finding is consistent with the literature [19].

The OCVs of all stack units and cells were greater more than 1.1 V. This result represents the excellent sealing achieved in the stack in addition to the lack of fragmentation in the cell electrolyte, indicating that these factors are not contributors to cell degradation inside the stack during operation in the current work. The morphology of the contact trace was found to remain on the cell anode and cathode at the interconnect channel tip, as shown in Figures 8–10. Figure 8 shows the morphology of the contact trace left on the anode side by the interconnect. Many regular and visible craters can be observed on the anode sides of cells A and B. Hence, the contact between the interconnect and the cell anode is not considered to be the main factor affecting cell degradation. Figures 9 and 10 present the morphology of the contact traces left by the interconnect on the cathode side of cells A and B in stacks 1 and 2, respectively. There are also many visible and

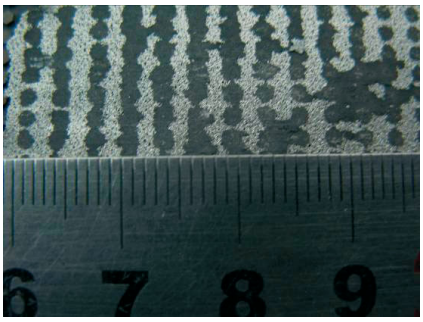

Fig. 8 Contact traces on cell anode sides after testing in stack 1 and stack 2.

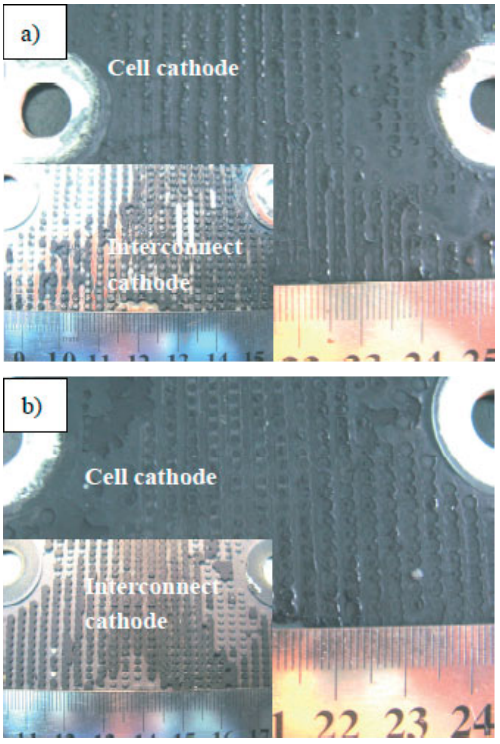

Fig. 9 Contact traces on cell cathode sides after testing in stack 1: (a) cathode side of cell A and interconnect B, and (b) cathode side of cell B and interconnect C.

regular craters on the cathode side of the cell, left by the interconnect tip used in stack 1. The traces left on the cathode side of interconnect B are somewhat different from those of interconnect C. The traces on interconnect B appear less distinct than those on interconnect C. Because the traces on interconnect C are slightly stronger than those on interconnect B, the contact between the cathode side of cell A and interconnect B is inferred to be slightly worse than that between the cathode side of cell B and interconnect C. Accordingly, the slight difference in contact traces leads to a degradation rate difference of approximately 0.15% per 100 h. Therefore, the interconnect coating can further improve the contact between the cell cathode side and the interconnect channel tip when the latter is embedded properly into the cathode current-collecting layer. In stack 2, visible craters also can be found on the cathode side of cell A with a corresponding degradation rate of 0.25% per 100 h. An insignificant contact trace can be identified on

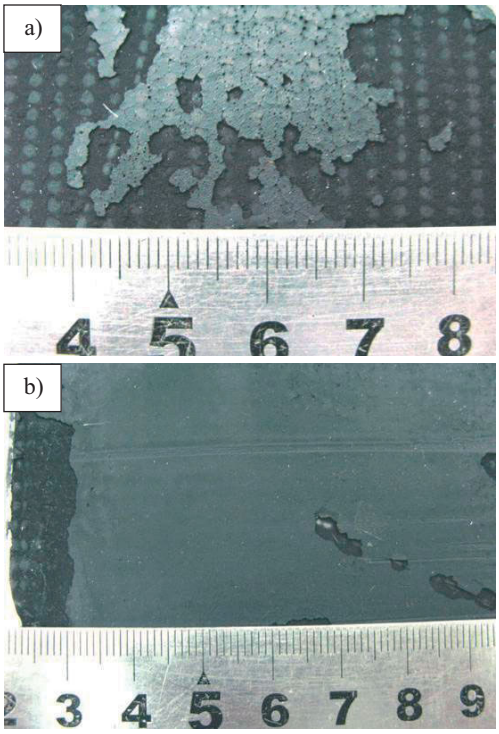

Fig. 10 Contact traces on cell cathode sides after testing in stack 2: (a) cathode side of cell A and (b) cathode side of cell B.

the cathode side of cell B with a corresponding degradation rate of 2.27% per 100 h. Hence, it can be concluded that the contact between the cathode current-collecting layer and the interconnect channel tip is the primary factor affecting the cell degradation inside SOFC stacks during operation.

Given the better contact between the cathode current-collecting layer of cell A and interconnect B than that between the cathode current-collecting layer of cell B and interconnect C in stack 2, the degradation rate of stack unit 1 is significantly lower than that of stack unit 2. Therefore, because the stack is well sealed, the stack degradation primarily depends on the contact between the cathode current-collecting layers and the interconnects. Interestingly, the contact between the cathode current-collecting layer and the interconnect is also a significant factor in the stack output power density, as found in our previous study [26]. By combining our previous results with the findings of the current work, the stack output performance (including the output power density and the stack degradation) can be significantly improved in planar SOFCs by enhancing the contact between the cell cathode-current collecting layer and the interconnect.

3.2 Stack Degradation During Thermal Cycling

A new two-cell stack, assembled as shown in Figure 1, was operated under nine thermal cycles (in the range of 750–200 °C) for 550 h. The degradation curves of the stack and stack units are shown in Figure 11a and b. The stack degradation rate was found to be 10.2% over nine thermal cycles (i.e., a degradation of 1.13% per cycle). The degradation rates of

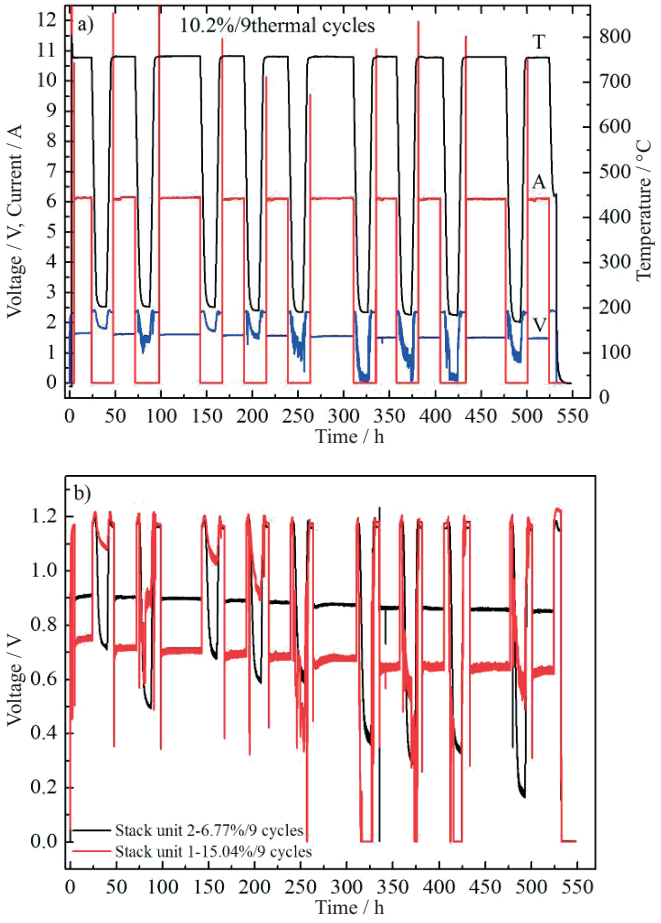

Fig. 11 Degradation of stack and its stack unit under thermal cycles: (a) stack and (b) stack unit.

stack units 1 and 2 were 6.77% per nine cycles and 15.04% per nine cycles, respectively. The degradation rate of stack unit 1 was twice that of stack unit 2. The OCV of the stack unit remained above 1.1 V under the thermal cycling conditions, indicating that stack degradation is independent of both gas leakage and microcracks in the cell electrolyte. The cell degradation curves of the stack are shown in Figure 12a. The degradation rates of cells A and B were 5.56% of nine cycles (0.62% per cycle) and 6.41% of nine cycles (0.71% per cycle), respectively. Compared with the results presented in Figure 11b, differences of 1.05% per cycle and 0.04% per cycle were obtained for the degradation rates of cells A and B, respectively.

Figure 12b presents the voltage drop caused by the interconnect under the thermal cycling conditions. Curve ❶ denotes the temperature, curve ❷ denotes the drop voltage caused by interconnect C, curve ❸ denotes the current discharge, and curve ❹ denotes the voltage drop caused by uncoated interconnect B. The voltage drop caused by coated interconnect C increased from 2 mV to approximately 20 mV after nine thermal cycles, i.e., 2 mV per cycle. The corresponding ASR of the coated interconnect increased from 20 to 200 mΩ cm^{-2} during the whole thermal cycling operation. The sum of the voltage drop caused by interconnect C and

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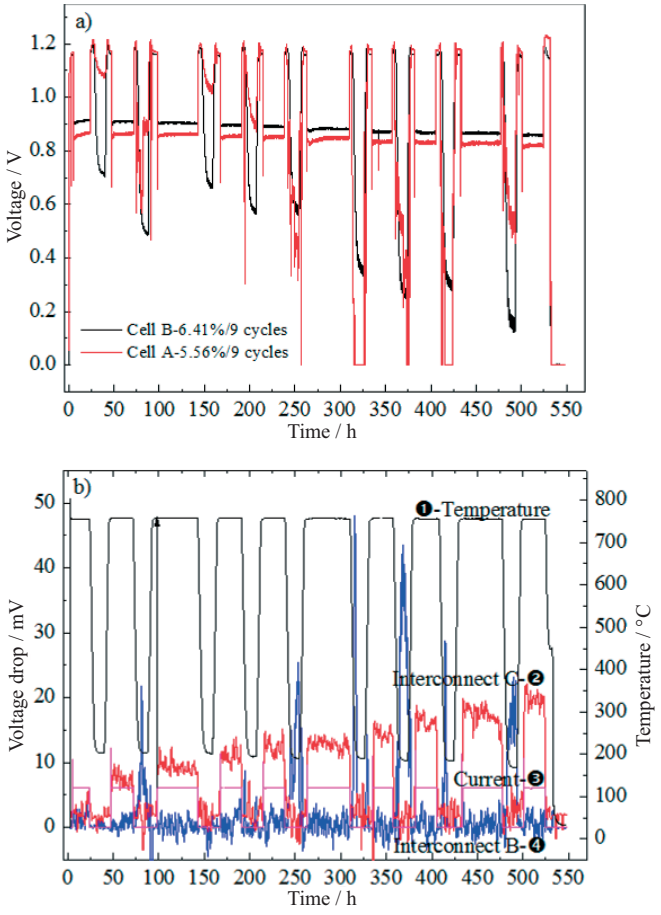

Fig. 12 Cell degradation and voltage drop caused by interconnect under thermal cycles: (a) cell degradation and (b) voltage drop curves caused by uncoated interconnect B-curve ❹ and by coated interconnect C-curve ❷, current – curve ❸, and temperature – curve ❶.

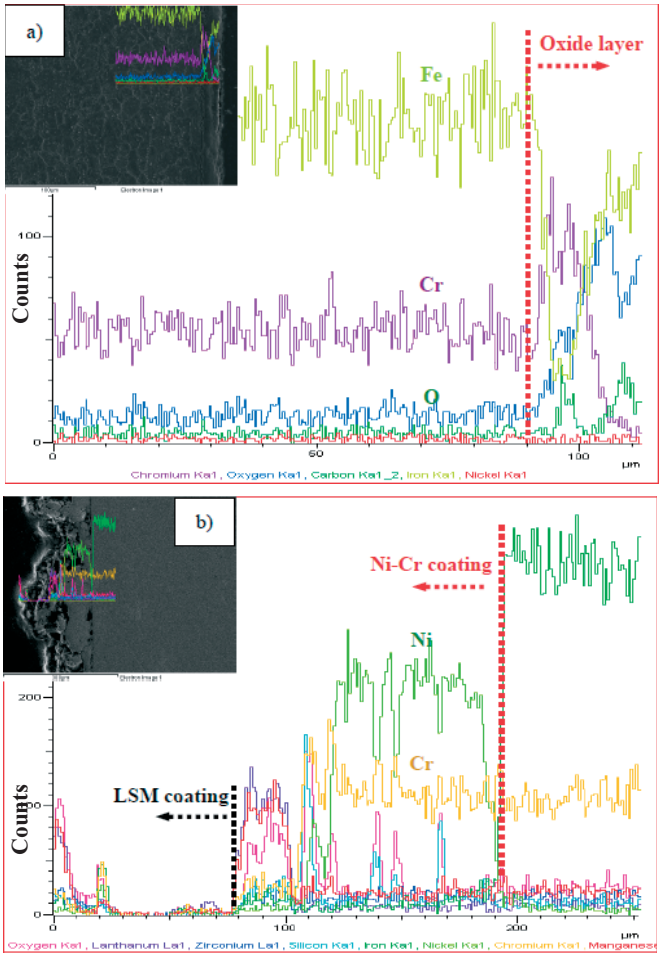

Fig. 13 EDS line on cathode side of interconnect: (a) uncoated interconnect B and (b) coated interconnect C.

cell B is approximately equal to that of stack unit 2. Hence, the degradation of stack unit 2 is independent of the contact between the cell electrode and the interconnect but is primarily dependent on the degradation of the cell itself as well as the voltage caused by coated interconnect C. Cell degradation may be affected by changes in the microstructure during thermal cycling. The voltage drop caused by interconnect B during the thermal cycling experiments was <2 mV. The corresponding ASR of interconnect B was calculated to be 20 mΩ cm^{-2} throughout the entire operation.

The degradation rate of cell A was slightly lower than that of cell B, as observed in Figure 12a. Stack degradation under stable operating conditions has no direct relation to Cr vaporization from the coated and uncoated interconnect, as demonstrated above. This conclusion can be verified again under the application of thermal cycling conditions to the SOFC stack, as represented in Figures 13 and 14 and Tables 5–7. The degradation of stack unit 1 is significantly different from that of cell A, likely because of the high-temperature oxidation applied to interconnect B as well as the differences in contact between the cell electrode and the interconnect. However, the voltage drop caused by interconnect B was approximately zero during the operation depicted in Figure 12b. Therefore, it can be concluded that the degradation of stack unit 1 was mainly induced by the contact between the cell electrode and the interconnect and is independent of the high-temperature oxidation of the interconnect itself. This result is largely due to oxidation of the interconnect, which was found to be insufficient to increase the ARS.

The morphology of the contact traces on the cell anode and cathode remaining from the interconnect channel tip was also investigated after thermal cycling. The morphology of the contact traces on the cell anode side during thermal cycling was the same as that resulting from long, stable operating conditions, as depicted in Figure 8. This similarity indicates that the cell anode side of the stack is strongly correlated to the interconnect channel tip. The morphology of the contact traces on the cathode side of cell A and interconnect B can be observed in Figure 15. The shape and size of the contact craters on the cathode side of cell A were almost identical to those at the channel tip of the interconnect. A depth of approximately 100 µm was found for the contact craters left by interconnect B, as shown in Figure 15a. Before contact with the cell electrode was established, the interconnect channel tip was thoroughly cleaned. After contact was established,

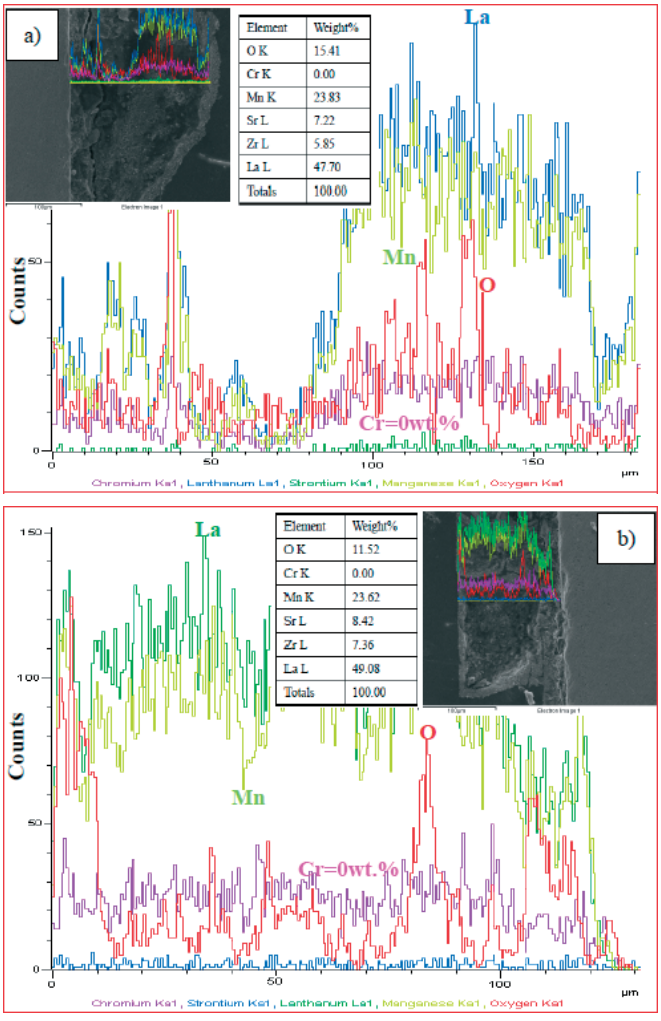

Fig. 14 EDS line in cell cathode: (a) cell A and (b) cell B.

Table 5 Main element in oxidation layer of uncoated interconnect B.

Elements	Fe	Cr	Mn	Si	Others
Wt.%	92.1	7.24	0.51	0.12	0.03

Table 6 Main element in coated layer of coated interconnect C.

Elements	La	Sr	Mn	Ni	Cr
Wt.%	49.9	26.4	11.2	8.44	3.73

Table 7 The content of Cr element in various cathode layer for cells A and B.

Cells	A / wt.%	B / wt.%
Active layer	0.048	0.025

a shallow trace on the interconnect channel tip was left by the cathode current-collecting layer. The morphology of the contact craters on the cathode side of cell B and coated interconnect C is shown in Figure 16. The shape and size of the contact craters on the cathode side of cell B left by interconnect C were slightly smaller than those of the interconnect channel tip. The contact craters were also regular and deep with a thickness of approximately 100 µm. The differences between the contact morphologies of interconnects B and C are because the latter was covered with a uniformly thick cathode

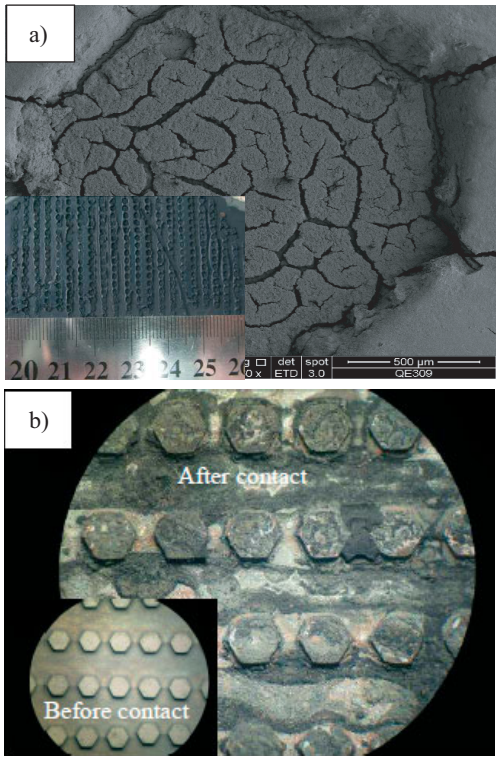

Fig. 15 Contact traces on cathode side of cell A and uncoated interconnect B: (a) cathode side of cell A and (b) cathode side of interconnect B.

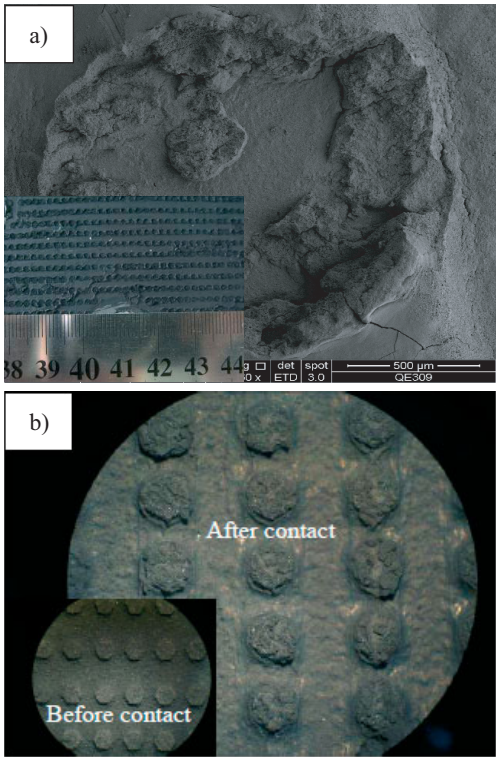

Fig. 16 Contact traces on cathode side of cell B and coated interconnect C: (a) cathode side of cell B and (b) cathode side of interconnect C.

current-collecting layer. The effective contact between the cathode current-collecting layer and interconnect B was less

well established than that between the cathode current-collecting layer and interconnect C. This difference indicates that the coating used on the interconnect can improve the interfacial contact between the cell cathode and the interconnect. This improvement decreases the stack degradation rate, which is caused by the deeper contact craters left by the uncoated interconnect during thermal cycling.

4 Conclusions

The ASR of the uncoated Fe–16Cr alloy interconnect in planar SOFC stacks was found to remain constant at approximately 20 mΩ cm^{-2} under both stable operating conditions at 750 °C and thermal cycling from 750 to 200 °C. This stability indicates that the oxidation layer present on the uncoated interconnect has a moderate and stable electrical conductivity, such that high-temperature oxidation does not increase the ASR during stack operation. The ASR of the coated interconnect also remained unchanged during long stable operating conditions at 750 °C, whereas the voltage drop caused by the coated interconnect increased from 20 to 200 mΩ cm^{-2} from 750 to 200 °C after nine thermal cycles.

Cell degradation inside SOFC stacks was found to depend primarily on the contact between the cathode current-collecting layer and the interconnect under both the thermally stable operating conditions at 750 °C and thermal cycling from 750 to 200 °C. However, cell degradation inside SOFC stacks was also found to be independent of both Cr vaporization from the Fe–16Cr alloy interconnect and high-temperature oxidation when the stack is sealed well. The coating on the interconnect can further improve the contact between the interconnect channel tip and the cell cathode current-collecting layer, given that a good contact exists for the interfaces under long stable operating conditions and thermal cycling conditions.

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